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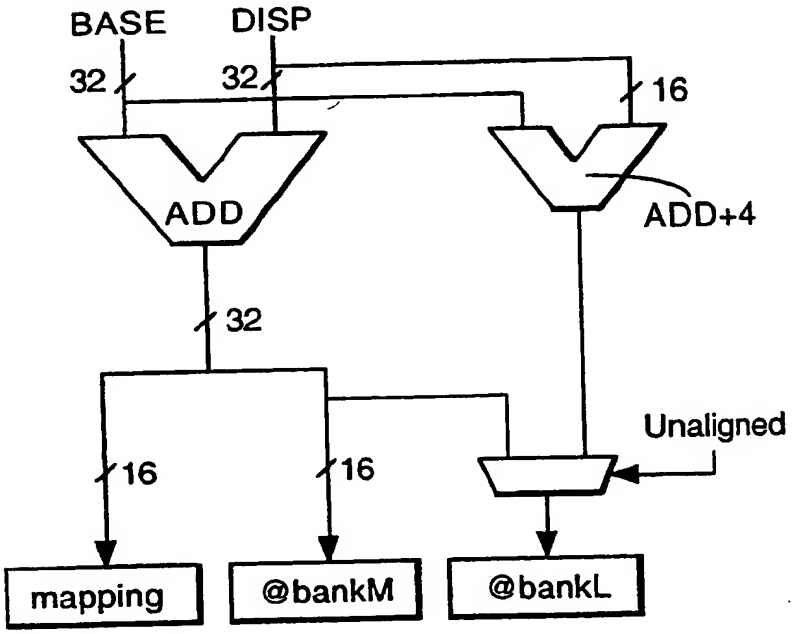
(54) Computer memory access

(57) A computer memory has at least two memory banks each having respective access circuitry and a memory capacity of half a word at each word address, the memory addressing circuitry providing an address to two memory banks simultaneously with adder circuitry to add to a word address for one of the banks a number equal to the number of bytes in a word thereby accessing two unaligned half words from respective memory banks.

Fig.2.



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used in accordance with the invention.

[0014] The particular example shown in Figure 1 illustrates a computer system used as a digital signal processor (DSP). Instructions are held in a program memory 11 and fetched by a control unit 12 which includes a decoder as well as a microinstruction generator. The microinstructions are output by a dispatch circuit 13 along line 14 to either a data unit 15 of an address unit 16 coupled in parallel. The data unit 15 and address unit 16 each include an execution pipeline 17 arranged to execute instructions in parallel using a data memory 20. The data unit 15 may itself include two parallel execution pipes receiving instructions from a data instruction queue 21 and accessing a common data register file 22. The address unit 16 may also include two parallel execution pipes accessing a common pointer register file 23 and receiving instructions from an instruction queue 24. Execution of instructions in the address unit will result in the generation of an effective address (EA) 24 for use in memory accessing as well as an OP code 25 and byte enable signals 26 for use in the memory accessing. The effective address is provided as an output of an address controller 32.

[0015] By arrangement of the data unit 15 and address unit 16 in parallel, the two units may simultaneously execute instructions thereby providing an access decoupled system providing improved efficiency in data manipulations involving the memory 20. The system may also incorporate an external system memory 30. Both memory 20 and the system memory 30 are coupled to a data memory interface 31. The effective address 24 generated by the address unit 16 may provide access to the system memory 30 or to the local memory 20. Access will be controlled by the memory interface 31.

[0016] In this particular case the local memory 20 consists of two parts. A first part is indicated as an X memory 34 and a second part consists of a Y memory 35. The X memory and Y memory are similarly constructed and each consists of an M bank 40 and an L bank 41. The M bank 40 has its own addressing circuitry 42 and a data storage region 43. Similarly the L bank has its own addressing circuitry 44 and its own data storage region 45.

[0017] Accesses to the X and Y memories 34 and 35 are controlled by timing signals from a clock 53 coupled to the memory interface 31 and the memory banks so that memory accesses are operated on clocked cycles.

[0018] The address controller 32 of the address unit 16 is shown in more detail in Figure 2 but will be described in more detail later. Firstly, the system of data storage in the regions 43 and 45 of the X and Y memories 34 and 35 will be described in more detail. Data is stored in the memory in bit sequences forming words, each word consisting of a multiple number of 8 bit sequences or bytes. In this particular example the word-length used is 32 bits but other examples may consist of 16 bits or 64 bits or any other multiple number of bytes for each word. The present example using 32 bits in each word is shown in Figure 3. Each word boundary in the memory is designated by a respective memory address and the word boundary commences with a designation of bit 0. In Figure 3 the example 50 indicates a single byte beginning at a word boundary 0 and extending to bit position 7. Example 51 illustrates a half word of data located adjacent a word boundary and the half word extends between bits 0 and 15. Example 52 comprises a whole word beginning at a word boundary and extends from bit 0 to bit 31. Example 52 does form an aligned word in that the entire word extends for 32 bits from a single word boundary.

[0019] The present example does however permit ready access to an unaligned word. That is a word consisting of two half words which are not located at a single word boundary. Furthermore it permits access to such an unaligned word in a single memory access cycle.

[0020] To achieve effective unaligned word access, the X memory 34 and the Y memory 35 are each divided into the two banks 40 and 41. Each bank is arranged to hold only a half word of data at each addressed location. Figure 5 shows four different memory access operations with each pair of memory banks 40 and 41. In diagram (a) four addressable rows are shown for each memory bank each row having a distinctive effective address. Each memory bank provides two bytes of memory capacity in each row. To achieve a single byte access, the address circuitry 42 and 44 of the two memory banks must be provided with the same word address thereby identifying the required row of memory together with the appropriate byte enable signals to select the required byte from the two memory banks. In the case of diagram (a) in Figure 5 byte 60 can be selected by addressing the top row of memory and providing a byte enable signal solely in the 00 byte position of bank 41 and no byte enable signals for the other three byte positions. Similarly bytes 61, 62 or 63 can be selected by addressing the correct word boundary and providing the required single byte enable signal for that word so that the single byte location is accessed. Each of those bytes would be accessed by a separate access cycle so that four successive access cycles would be needed to access the four separate bytes shown in diagram (a). In diagram (b) two half words are shown each occupying two adjacent byte locations. Half word 65 is located in the L bank 41 whereas half word 66 is located in the M bank 40. They are located in positions relating to different word boundaries and they may be accessed in two successive cycles. The first cycle will access the word boundary containing half word 65 and the byte enable signals will be set for the two bytes in bank 41 but not set for memory bank 40. In the next memory access cycle the word boundary address is that containing the half word 66 and the byte enable signals are set for memory bank 40 but not set for memory bank 41. In this way, each memory access cycle accesses the required half word. For accessing a normally aligned word, the operation is

space.

[0027] The invention is not limited to the details of the foregoing example.

Claims

1. A computer system comprising instruction supply circuitry, a plurality of parallel instruction execution pipelines, a read and write memory, a memory addressing circuitry for addressing said memory as a result of instruction execution in said pipelines, wherein said memory is arranged to hold data in addressable words each comprising a plurality of bytes forming two half words, said memory addressing circuitry being operable to provide successively a plurality of word addresses and said memory comprising two memory banks each having respective access circuitry for the same word addresses and a memory capacity of half a word at each word address, said memory addressing circuitry having address output circuitry to provide an address to both memory banks simultaneously and adder circuitry to add to a word address for one of the banks a number equal to the number of bytes in a word, the address output circuitry thereby being selectively operable to access in a single access cycle two unaligned half words from respective memory banks at adjacent word locations in the two memory banks.

2. A computer system according to claim 1 in which said memory addressing circuitry is arranged to separate each word address into a first set of bits identifying a memory region provided by said two memory banks and a second set of bits identifying a memory address within said memory banks, said adder being arranged to receive said second set of bits and selectively add said number to said second set of bits.

3. A computer system according to claim 2 in which said second set of bits comprise the least significant half of the bits of the memory address.

4. A computer system according to any one of the preceding claims in which said one of said memory banks is connected to a multiplexer having two inputs, one input being an output from said adder and a second input being the address supplied to the other memory bank, whereby selective operation of the multiplexer permits access to an aligned word or an unaligned word in the two memory banks.

5. A computer system according to any one of the preceding claims in which said memory addressing circuitry is operable to provide byte enable signals to indicate which bytes at each word address are to be accessed, and said access circuitry of each memory bank is arranged to receive said byte enable signals to access selected bytes at each word location addressed in the memory banks.

6. A computer system according to any one of the preceding claims including timing circuitry to control access to each memory bank simultaneously in successive access cycles, said memory addressing circuitry being operable to access either aligned or unaligned words in the same access cycle.

7. A method of accessing memory in a computer system having a memory arranged to hold data in addressable words each comprising a plurality of bytes forming two half words, said method comprising dividing the memory into two memory banks each having respective access circuitry for the same word addresses and a memory capacity of half a word at each word address, generating a single address for use in addressing both memory banks simultaneously, adding to said address a number equal to the number of bytes in a word to form an incremented address and selectively supplying said address to one memory bank and said incremented address to the other memory bank thereby to access in the same access cycle half words from respective memory banks forming an unaligned word.

8. A method according to claim 7 in which said address comprises only the least significant bits of a full word address, said bits being sufficient to identify the memory region provided by said memory banks and said number is added only to said least significant bits.

9. A method according to claim 7 or claim 8 in which byte enable signals are supplied to each memory bank to access selected bytes at each word location addressed in the memory bank.

Fig.2.

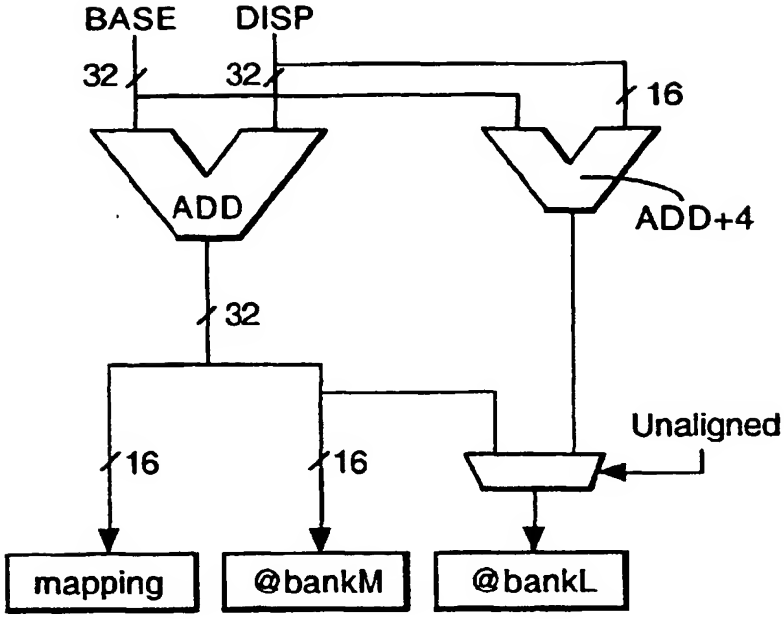
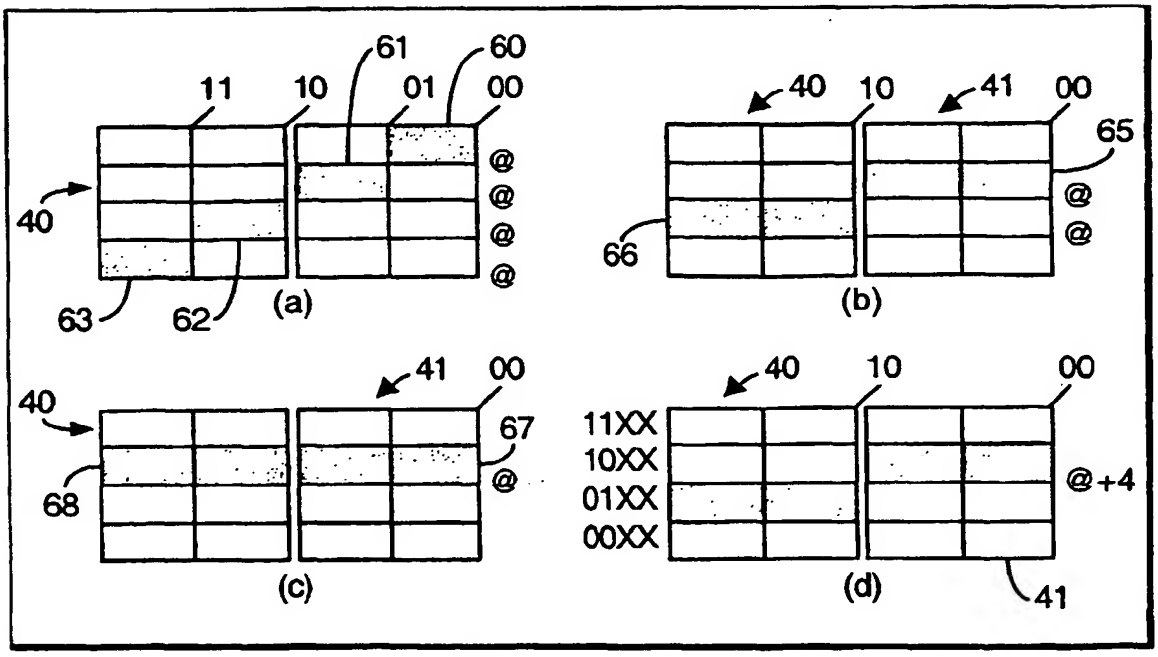


Fig.5.



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EUROPEAN SEARCH REPORT

Application Number
EP 99 41 0062

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
X	US 4 432 055 A (SALAS EDWARD R ET AL) 14 February 1984 (1984-02-14)	1-3,5-9	G06F12/04 G06F9/34
A	* column 15, line 60 - column 20, line 52 *	4	G11C8/00
X	US 4 247 920 A (SPRINGER RICHARD A ET AL) 27 January 1981 (1981-01-27)	1,6,7	
A	* the whole document *	2-5,8,9	
A	PATENT ABSTRACTS OF JAPAN vol. 012, no. 119 (P-689), 14 April 1988 (1988-04-14) & JP 62 245351 A (HITACHI LTD;OTHERS: 01), 26 October 1987 (1987-10-26) * abstract *	1,7	
A	US 5 806 082 A (SHAW JENG-JYE) 8 September 1998 (1998-09-08) * column 3, line 63 - column 4, line 49 *	1-9	
A	WO 99 14666 A (SIEMENS MICROELECTRONICS INC) 25 March 1999 (1999-03-25) * the whole document *		TECHNICAL FIELDS SEARCHED (Int.Cl.7) G06F G11C

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	4 November 1999	Daskalakis, T

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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D : document cited in the application
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